PERFORMANCE →

A is X times faster if
$Lat(P,A) = \frac{Lat(P,B)}{X}$

$TP(P,A) = X \cdot TP(P,B)$

& A is X% faster if
$Lat(P,A) = \frac{Lat(P,B)}{(1+\frac{X}{100})}$

$TP(P,A) = TP(P,B) \cdot (1+\frac{X}{100})$

$TP(P1+P2,A) = \frac{2}{[TP(P1,A)]^{-1} + [TP(P2,A)]^{-1}}$

Arithmetic → $\frac{1}{N}\sum_{1}^{N} Lat(P)$

Harmonic → $\frac{N}{\sum_{1}^{N} \frac{1}{TP(P)}}$

Geometric → $\sqrt[N]{\prod_{1}^{N} Sn(P)}$

Amdahl's Law →

$S = \frac{1}{(1-f) + f/N}$

Iron Law →

$\frac{Instn}{Prog} \times \frac{Cycle}{Instn} \times \frac{Second}{Cycle} = \frac{Seconds}{Prog}$

DIC | CPI | period or F^{-1}

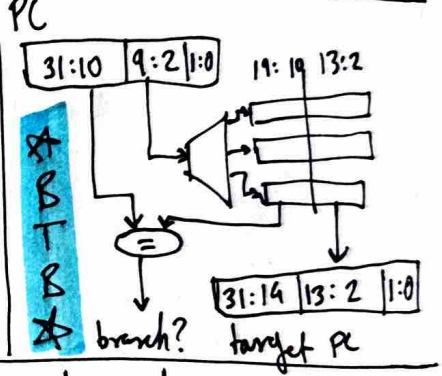
BYPASSING →

☆ Always assume writeback in first half, decode in second half

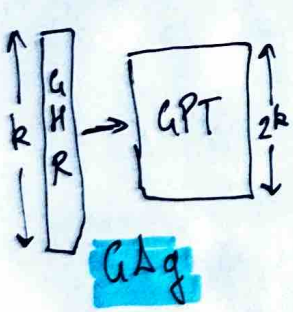
M→X, W→X, W→M lanes

DEPENDENCES →

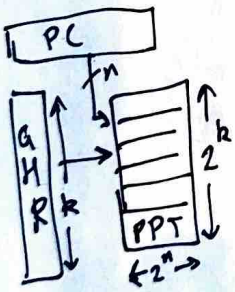
RAW → true dependence
WAR → anti dependence
WAW → output dependence
RAR → DNE ∅



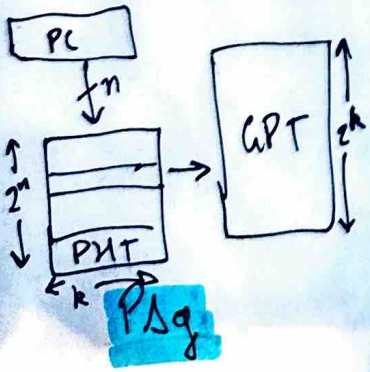
TWO-LEVEL PREDICTORS →



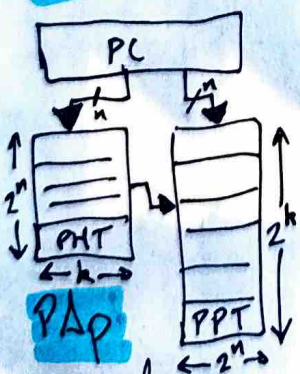
GAg



GAp



PAg



PAp

☆ When counting size, consider BOTH levels of predictors

☆ Hybrid (Tournament) Predictors

TOMASULO → ☆ copy-based renaming

① Check for CDB broadcast & see what hits
② Issue instructions as necessary
③ Update counter of executing instructions
④ Decode new instructions (if possible)

☆ In-order dispatch, out-of-order issue

REORDER BUFFER →

☆ Forwarding to younger instn → OoO
☆ Writeback to architectural reg → IO

W becomes
C → Complete
R → Retire

☆ Writeback & decode/issue can happen in the same clock cycle.

☆ MIPS R10K rolls back to last stage of instruction just before fault. Faulting instruction never executes.

☆ Fully set-associative – no index bits
Direct-mapped – zero associativity.

CACHES →

① Write thru → update next level imm on write
② Writeback → update only on replace/evict
③ Allocate → write requires loading first.
④ Non-allocate → write directly to next level

Cache Miss Types

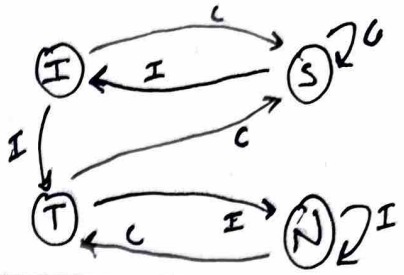
① Cold → would miss on ∞ cache, never seen
② Conflict → associativity low, Tot - Cold - Cap.
③ Capacity → cache too small, misses even in fully set-associative caches
④ Upgrade → miss due to delay to acquire write permissions
⑤ Coherence → miss due to invalidation

Increase in ABC

① Associativity → cold miss ↓
② Block size → cold miss ↕ conflict miss ↑
③ Capacity → capacity miss ↓

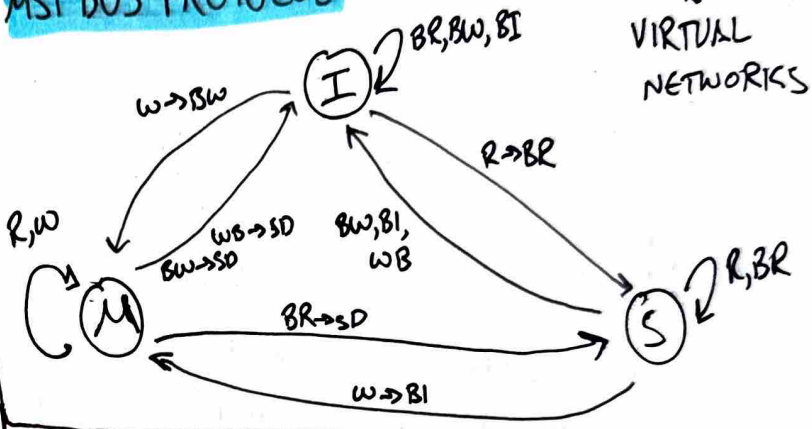
Stride Prefetcher FSM

Initial, Stable, Transient, Incorrect



MSI BUS PROTOCOL →

★ VIRTUAL NETWORKS



Flynn Taxonomy →

SIMD → DLP
SISD → ILP/pipelining
MIMD → TLP, SPMD
MISD → WASΔ?

Flynn Bottleneck

IPC = CPI = 1

TS → spins globally, creates traffic → coherence
TTS → spins locally, but others can own it
SC → returns 0 if store failed.