NMOS → degrades 1 by V_{tn}
PMOS → degrades 0 by $|V_{tp}|$

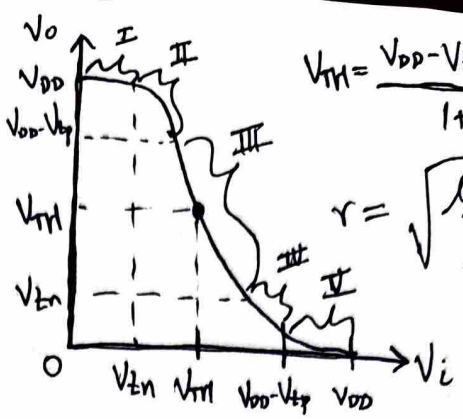
Layout layers →
① n-well ② poly
③ n+ diff ④ p+ diff
⑤ Contacts ⑥ Metal layer

	Cutoff	Triode	Active
C_{gb}	C_o	0	0
C_{gs}	0	$C_o/2$	$2C_o/3$
C_{gd}	0	$C_o/2$	0

$$\tau = \frac{RC(N+1)}{2N}$$

$$t_d = \frac{t_{df}+t_{dr}}{2} \qquad \left.\frac{W_p}{W_n}\right|_{opt} = \sqrt{\frac{\mu_n}{\mu_p}} \qquad N_D = \frac{L}{W}$$

$t_{dr} = 1.2 R_{eqp} \cdot C$
$t_{df} = 1.2 R_{eqn} \cdot C$
$R_{eq} = \frac{2.5}{\mu C_{ox}(W/L)(V_{sat}-V_t)}$



$$V_{TH} = \frac{V_{DD} - V_{tp} + V_{tn}\gamma}{1+\gamma}$$

$$\gamma = \sqrt{\frac{\mu_n (W/L)_n}{\mu_p (W/L)_p}}$$

Parallel → added length
Series → added width

Assume $\mu_n = 2\mu_p$
PMOS → L=2 R=1
NMOS → R=1, C=1

$$\frac{t_{df2}}{t_{df1}} = \frac{C_{L2}}{C_{L1}} \times \frac{(W/L)_{N1}}{(W/L)_{N2}}$$

$$\frac{t_{dr2}}{t_{dr1}} = \frac{C_{L2}}{C_{L1}} \times \frac{(W/L)_{P1}}{(W/L)_{P2}}$$

$NM_L = V_{OL} - V_{IL}$
$NM_H = V_{OH} - V_{IH}$

τ_{inv} is delay of FO1 w/no parasitic $\therefore \tau = 3RC$

If $\gamma = 1$ then $\tau = 2RC$ for FO1
If parasitic = gate C then $\gamma = p_{inv} = 1$

$C_j = \frac{C_{j0}}{(1+V_R/\phi)^M}$ C_j uses A
C_{jsw} uses P

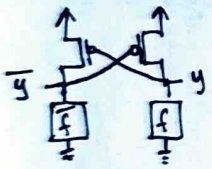
Elmore → $\tau_i = \sum_k C_{ik} R_{ik}$
Total → $N f \tau_{inv}$

$P_{DISS} = f C_L V_{DD}^2 P_{1\to 0}$
↳ Could be $V_{DD}(V_{on} - V_{OL})$

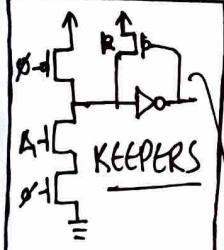
$P_{DP} = \frac{V_{DD} I_{pk}}{2}(t_r + t_f)(f) P_{1\to 0}$

① Velocity Saturation ($I_D \propto V_{GS}$)
② Channel length modulation
③ Body Effect
④ Subthreshold Conduction
⑤ Junction leakage current
⑥ Tunneling through oxide
⑦ Temperature
⑧ Geometry Dependence

★ Cascode does not draw static power

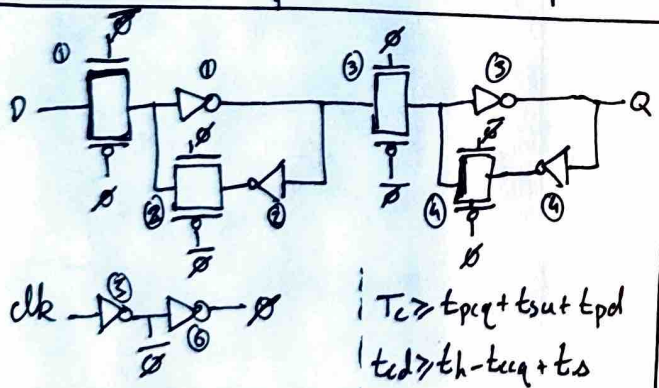


★ High & falling low never allowed
★ Footed allows CMOS to drive dynamic gates but inverted



Charge sharing
$V_x = V_y = \frac{C_y}{C_y + C_x} V_{DD}$
↳ k should be small
$\Sigma Q_{int} = \Sigma Q_{fin}$

Pros of footed:
① Input can be HIGH during precharge
② Better noise
③ Easier clocking
④ Reduced charge sharing



$T_c \geq t_{pcq} + t_{su} + t_{pd}$
$t_{cd} \geq t_h - t_{ccq} + t_s$

$t_{pcq} = I_5 + I_6 + T_{C3} + I_3$
$t_h = I_5 + I_6$
$t_{su} = T_{D1} + I_1 + I_2 - I_5$

Triode → $\beta[2(V_{GS})V_{DS} - V_{DS}^2]$
Saturation → $\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_S-V_{tn})^2$

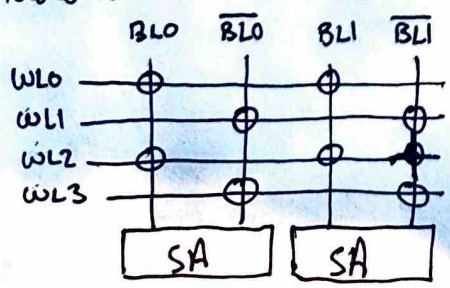
$R = \frac{\rho L}{A}$ $\quad Q = CV, I = \frac{Q}{t}, t = \frac{CV}{I}$

For finding W_n of inverters in a chain
↳ $W_n = \frac{C_{in}}{3L_n C_{ox}}$ → C_{in} is cap of previous state

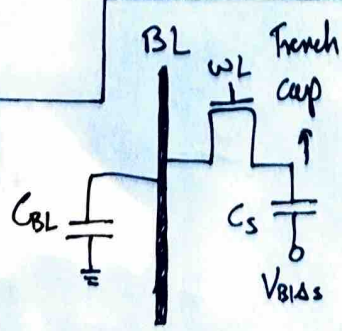
$MTBF = \frac{T_c e^{T_c/\tau_s}}{N t_{rd}} = \frac{k_1 e^{T_c/\tau_s}}{F_D F_{CLK}}$
$k_1 = [T_c]^{-1}$

$\Delta V_x = \frac{C_2}{C_1+C_2}\Delta V_a$
$V_{tn}' = \left(\frac{C_1+C_2}{C_2}\right)(V_{tn} - V_b)$

Folded Bitline Architecture



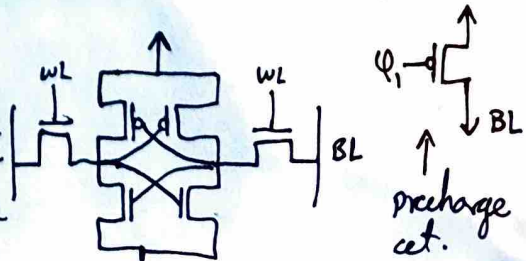
★ Bitline twisting ★



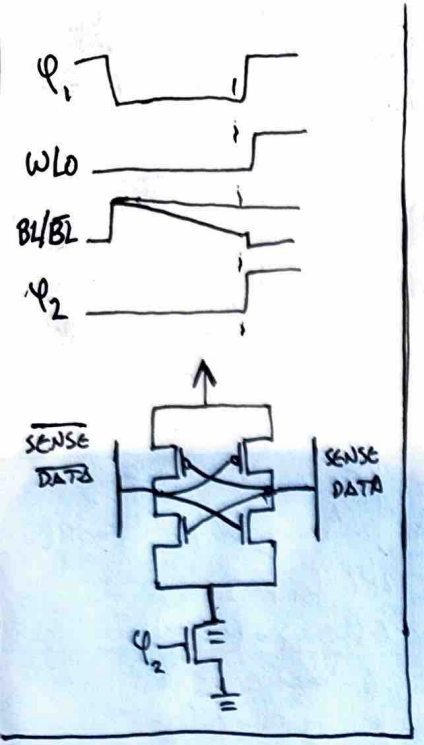
$\frac{1}{2}V_{DD} - \left(\frac{C_S}{C_{BL}+C_S}\right)\left(\frac{V_{DD}}{2}\right)$
ΔV

$W_1 \geq 1.3 W_3 \rightarrow RD$
$W_3 \geq 1.15 W_5 \rightarrow WR$
} set both to V_{tn}/V_{tp}

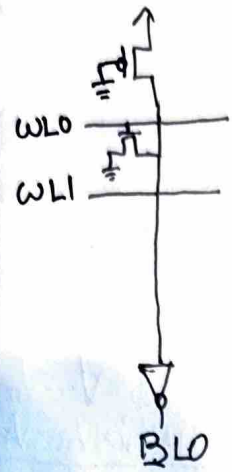
★ Draw circuit and write current equation



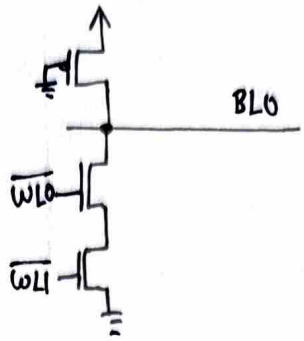
★ To write 1 raise BL high



NOR



NAND



★NOR is faster
but NAND is denser