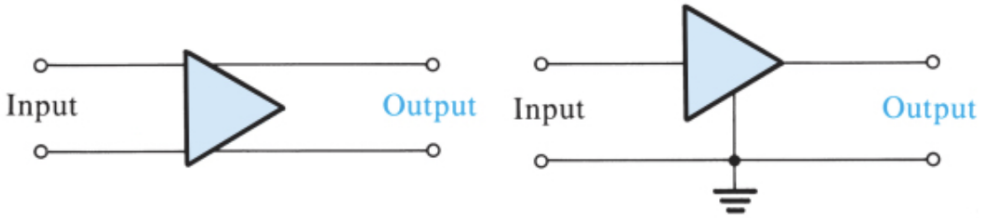
Signals and Amplifiers

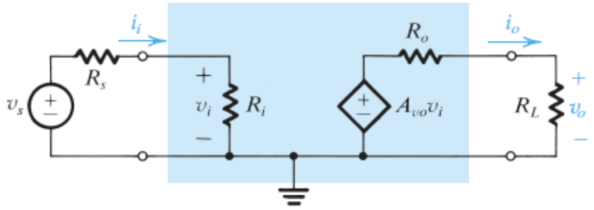
1.4 Amplifiers

- Simplest signal processing task is amplification — should be done linearly $v_o = Av_i$



1.5 Circuit Models for Amplifiers

1.5.1 Voltage Amplifiers



- Model consists of a VCVS with gain factor A_{vo}, an input resistance R_{in} to account for current being drawn from the source, and an output resistance R_{out} that accounts for change in voltage as current drawn by the load
  - To prevent losing gain, output resistance $R_o << R_L$
  - Thus A_v is the voltage gain of the unloaded amplifier, or open-circuit voltage gain.
- In some cases we are interested in a power gain over a voltage gain.
  - Connecting the source directly to the load would result in significant signal attenuation.
  - Amplifier would then need much higher input resistance and lower output resistance.

- Called a **buffer amplifier**

1.5.5 Determining R_i and R_o

- R_i determined by applying an input voltage v_i and measuring the current i_i.
- Output resistance R_o sound by eliminating the input signal source and applying a volage signal v_x to the output

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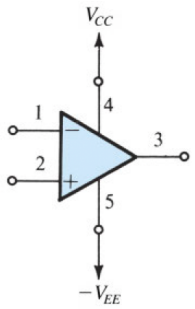
Operational Amplifiers

2.1 The Ideal Op Amp

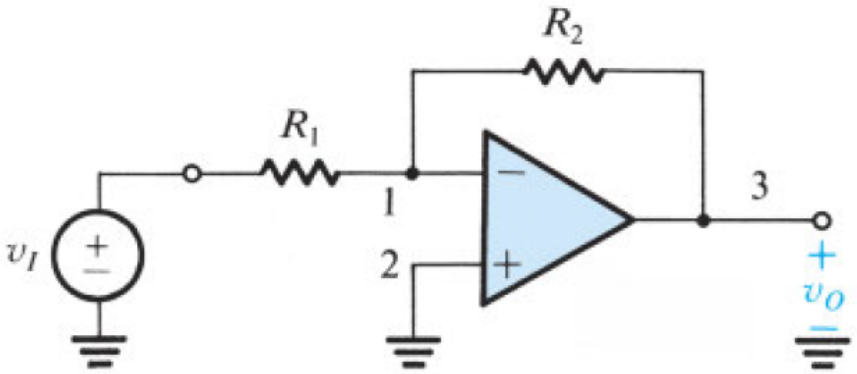
2.1.1 The Op-Amp Terminals



2.1.2 Function and Characteristics of the Ideal Op Amp

- Input impedance of an ideal op amp is supposed to be infinite ∞
- Output impedance of an ideal op amp is supposed to be zero.
- Terminal (1) is called the inverting input terminal and (2) is called the non-inverting input terminal.
- The op amp responds only to the difference signal $v_2 - v_1$ and ignores any signal *common* to both inputs — property called common-node rejection
- Ideal op amps will amplify signals of any frequency with equal gain, and are thus said to have infinite bandwidth.

2.2 The Inverting Configuration

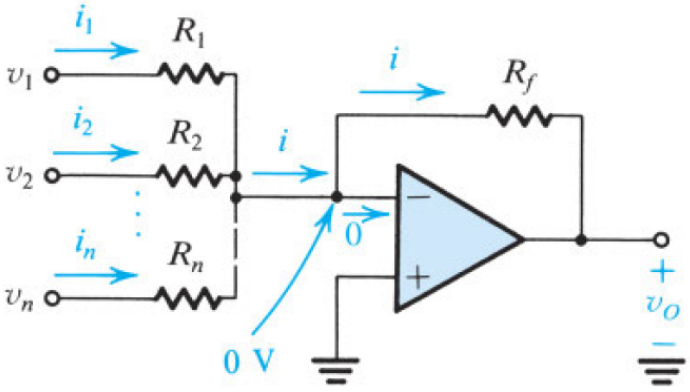


- Inverting configuration means connecting R_2 from output back to the inverting input terminal — applying **negative feedback**.
  - If R_2 was connected to terminal (2) instead, we would call it **positive feedback**, which would cause op amp to saturate

$$\frac{v_O}{v_I} = -\frac{R_2}{R_1}$$

$$R_i = R_1$$

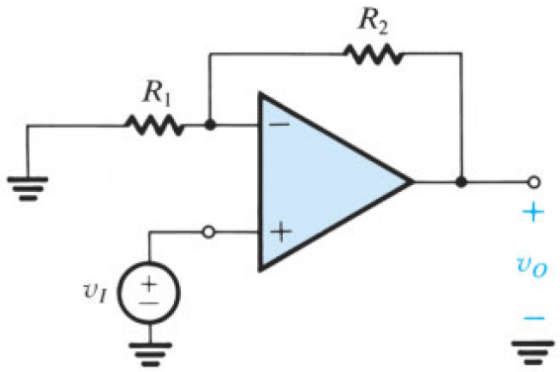
2.2.4 The Weighted Summer



$$v_O = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

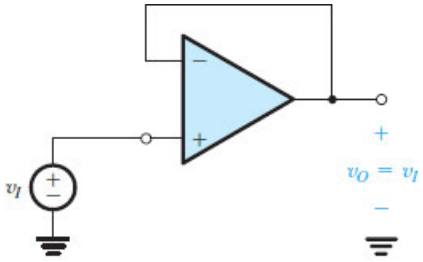
- Output voltage is a weighted sum of the input signals — therefore called a weighted summer.

2.3 The Non-Inverting Configuration



$$\frac{v_O}{v_I} = 1 + \frac{R_2}{R_1}$$

- Say v_I increases — such a change will cause v_{Id} to increase and v_O to increase as well
  - Portion of increase in v_O will feed back into inverting input terminal, counteracting the increase in v_{Id}, driving it back to 0.
  - This is called **degenerative feedback**.
- Input impedance is infinite and output resistance is zero.
- The voltage follower:



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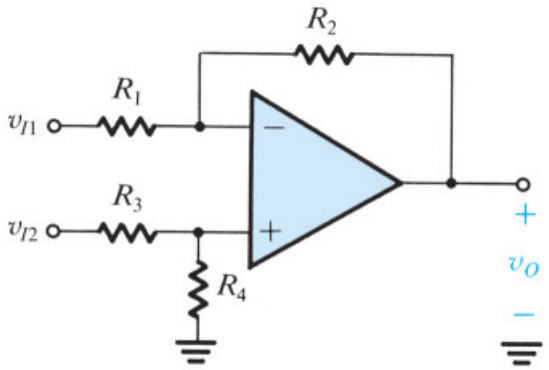
2.4 Difference Amplifiers

2.4.1 Single-Op-Amp Difference Amplifier



- Voltage divider ratio can be determined as:

$$\frac{R_4}{R_4 + R_3}\left(1 + \frac{R_2}{R_1}\right)$$

- We can satisfy this condition by selecting

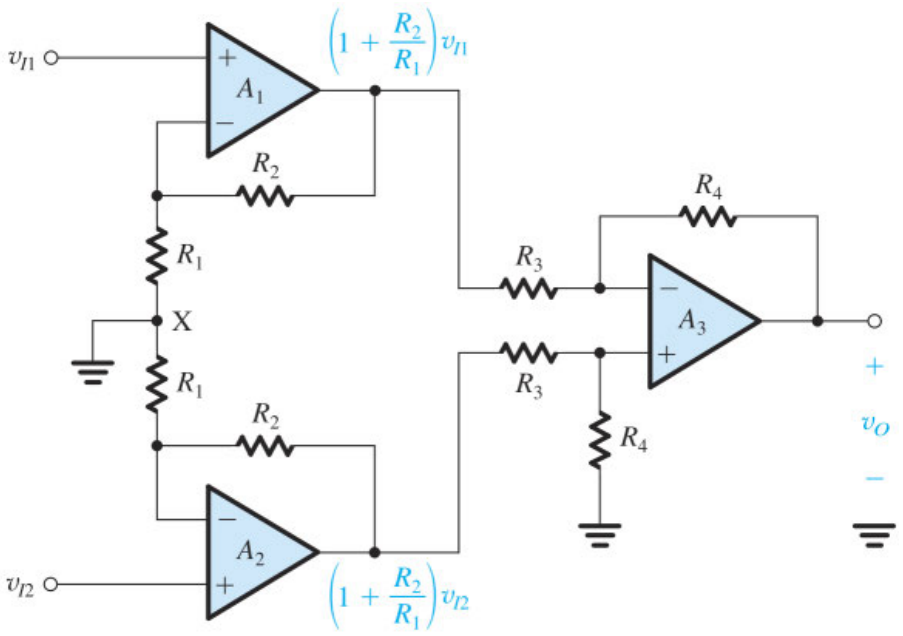
$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$

2.4.2 The Instrumentation Amplifier

- Low input resistance problem solved by using voltage followers t buffer input terminals.
- We can achieve high voltage gain from the buffers by using non-inverting stages over unity-gain followers
  - Does not compromise high input resistance.
- Differential amplifier then allowed to implement differencing function and reject common-mode signals

$$v_O = \frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right)$$

- Some disadvantages
  - Input common mode signal v_{Icm} amplified in the first stage by gain equal to that experienced by differential signal v_{Id} – could saturation the op amps
  - Amplifier channels in first stage have to be perfectly matched, otherwise a common-mode input signal will appear differently
    - Difference would then get amplified by the difference amplifier
  - To vary differential gain A_v the resistor values must vary simultaneously



(a)

2.5 Integrators and Differentiators

2.5.1 Inverting Configuration with General Impedance

- Consider replacing closed-loop configuration with impedances replacing resistors

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)}$$

2.5.2 The Inverting Integrator

- Place capacitor in feedback path and resistor at the input
- Input is a time-varying function, virtual ground at inverting op amp input causes $v_I(t)$ to appear across R, causing current
- current flows through capacitor C causing charge to accumulate.
  - Capacitor voltage will change by $\frac{1}{C}\int_0^t i_1(t)dt$

$$v_O(t) = -\frac{1}{CR}\int_0^t v_i(t')dt' - V_C$$

- Output voltage is proportional to time integral of the input with V_C the initial condition

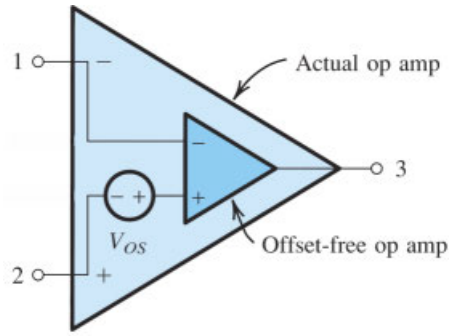
2.5.3 The Op-Amp Differentiator

$$v_O(t) = -CR\frac{dv_I(t)}{dt}$$

2.6 DC Imperfections

2.6.1 Offset Voltage

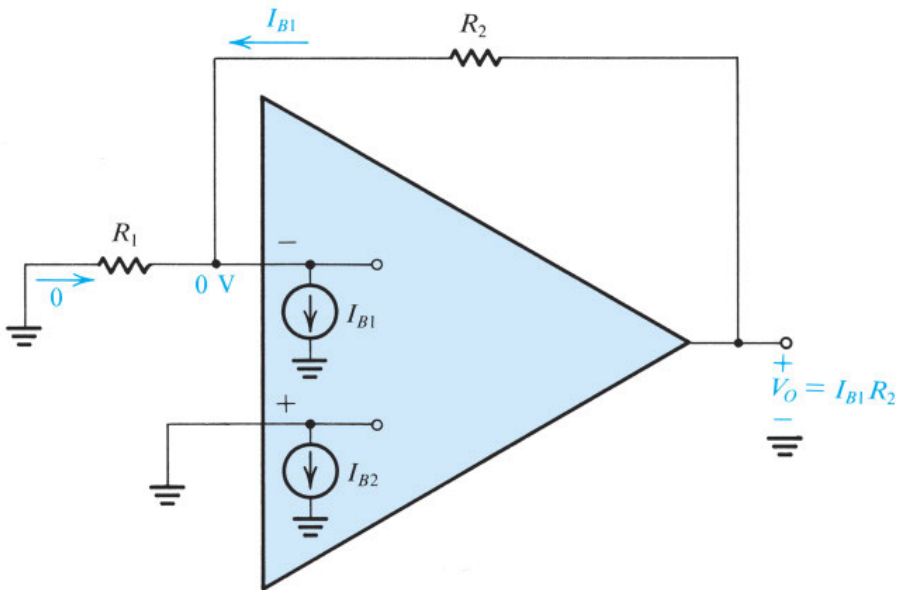
- If two input terminals of the op amp are tied together and connected to ground, we see that a finite DC voltage exists at the output.
  - If op amp has high DC gain, the output will be at high or low saturation point
  - Op amp can be supplied with an input offset voltage of appropriate polarity



2.6.2 Input Bias and Offset Currents

- Bias currents are independent of fact that real op amps have finite input resistance

$$I_B = \frac{I_{B1} + I_{B1}}{2}$$



2.8 Large-Signal Operation of Op Amps

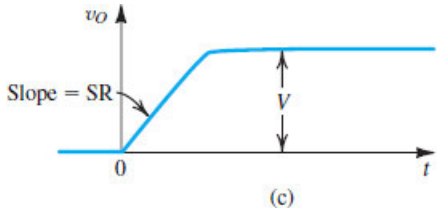
2.8.1 Output Voltage Saturation

- Op amps operate linearly over a limited range of values
- If an op amp powered by $\pm 15V$ saturates when output reaches $\pm 13V$ then we say that the rated output voltage is $\pm 13V$
- Op amps for which L_- and L_+ equal the supply voltages are called rail-to-rail output

2.8.3 Slew Rate

- There is a specific maximum rate of change possible at the output of a real op amp
- Called the slew rate

$$SR = \left.\frac{dv_o}{dt}\right|_{max}$$



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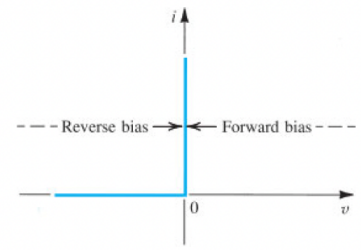
Diodes

4.1 The Ideal Diode

4.1.1 Current-Voltage Characteristics

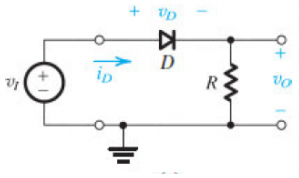
- Diodes are the most fundamental nonlinear circuit element.
- If a negative voltage is applied to the diode, no current flows and diode is **reverse-biased**. In this mode, the diode is **cut-off**, or just **off**.
- If a positive voltage is applied, then the diode is in **forward-bias** mode, turned **on**, or simply on.

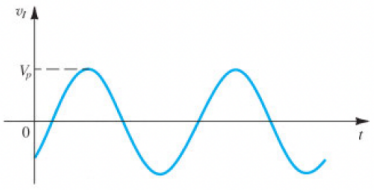


Ideal diode i-v characteristic

- Positive terminal called **anode** and negative terminal called **cathode**.

4.1.2 The Rectifier



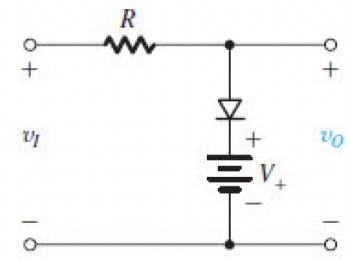


- The circuit above rectifies the signal and hence is called a rectifier. It can be used to generate DC from AC.

4.1.3 Limiting and Protection Circuits

- Diode current during conduction is given by

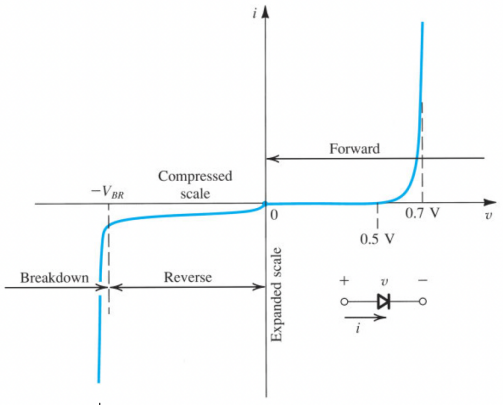
$$i_D = \frac{v_i - V_+}{R}$$



- Every complex circuit includes protection circuits that keep at-risk circuit nodes within safe limits. These are a class of limiters called electrostatic discharge (ESD) circuits.

4.2 Terminal Characteristics of Junction Diodes

- Characteristic curve consists of three distinct regions
  - The forward-bias region – $v > 0$
  - The reverse-bias region – $v < 0$
  - The breakdown region – $v < -V_{BR}$



4.2.1 The Forward-Bias Region

- In the forward-bias region, the $i - v$ region is closely approximated by

$$i = I_S(e^{v/V_T} - 1)$$

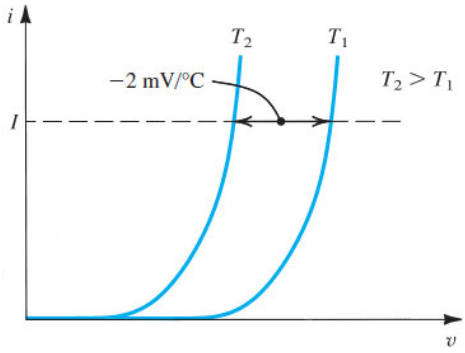
- The value I_S is called the saturation current.
- The voltage V_T is caleld the thermal voltage, given by $V_T = kT/q$, we usually go with $25mV$.

$$v = V_T \ln \frac{i}{I_S}$$

$$\frac{I_2}{I_1} = e^{(V_2 - V_1)/V_T}$$

- We can rewrite this as:

$$V_2 - V_1 = V_T \ln \frac{I_2}{I_1}$$



4.2.2 The Reverse-Bias Region

- When the applied voltage is negative and a few times bigger than V_T, we can say that $i \approx -I_S$

4.2.3 The Breakdown Region

- The diode enters the breakdown region when the magnitude of the reverse voltage exceeds a threshold value that is specific to the particular diode, called the **breakdown voltage**, denoted V_{BR}.

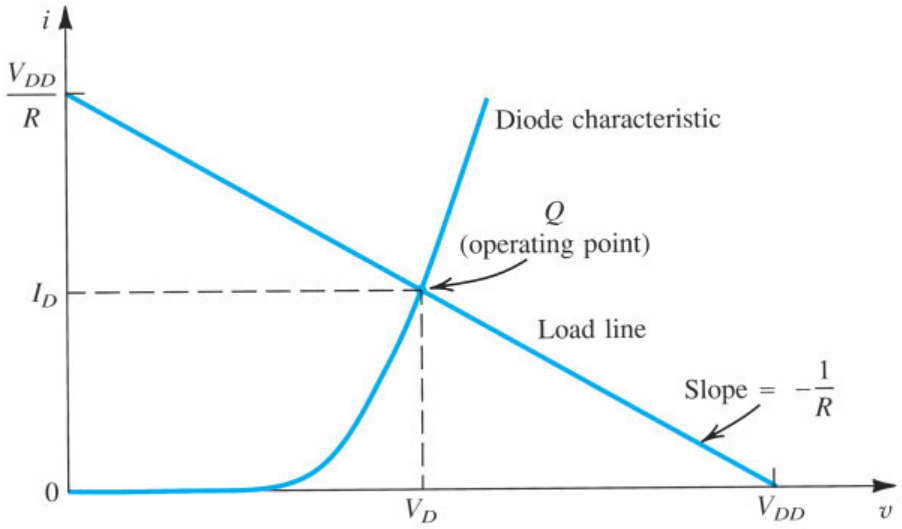
4.3 Modelling the Diode

4.3.1 The Exponential Model

$$I_D = I_S e^{V_D/V_T}$$

$$I_D = \frac{V_{DD} - V_D}{R}$$

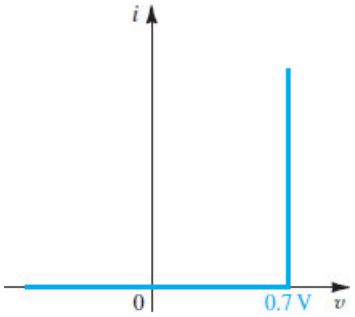
4.3.2 Graphical Analysis Using the Exponential Model



4.3.3 Iterative Analysis Using the Exponential Model

- Use the exponential and Ohm's Law equations in turn to solve for current and voltage.

4.3.5 The Constant-Voltage-Drop Model



(b)

4.3.6 The Ideal-Diode Model

- Voltage drop across diode is $0.7\,V$ when voltage applied is positive.

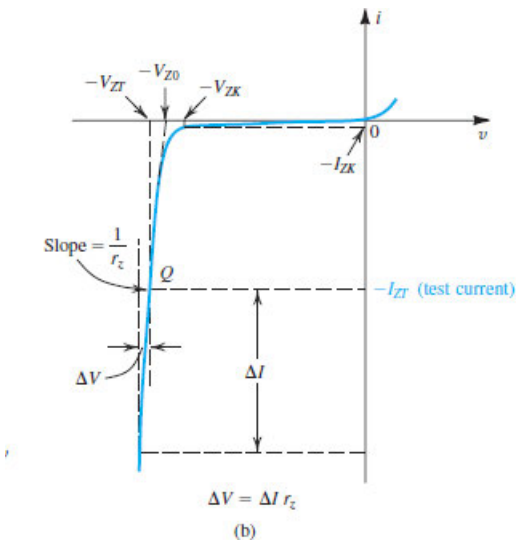
4.3.7 Operation in the Reverse Breakdown Region

Avalanche Breakdown

- Observed when $V_{BR} > 10V$.
- Large reverse current with high V_{BR} results in high power dissipation.

Zener Breakdown and the Zener Diode

- Zener diodes maintain a nearly constant reverse voltage drop, V_Z over a wide range of reverse currents.



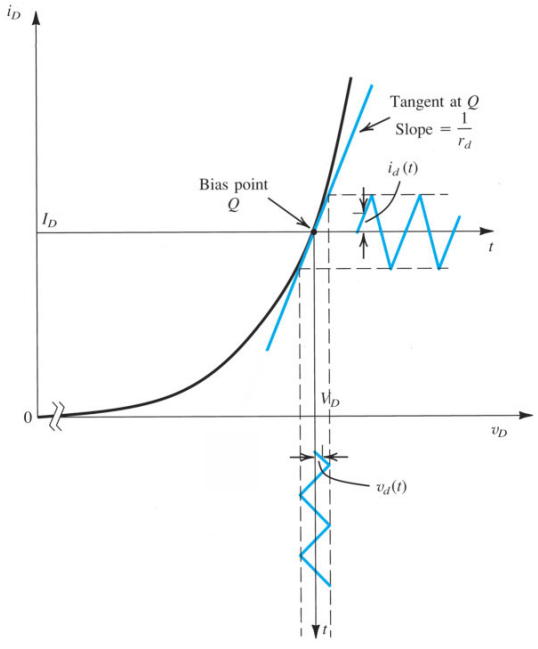
- Equivalent circuit model given by $V_Z = V_{Z0} + r_z I_Z$

4.4 The Small-Signal Model

$$v_D(t) = V_D + v_d(t)$$

$$i_D(t) = I_S e^{v_D/V_T}$$

$$i_D(t) \approx I_D(1 + v_d/V_T)$$



- There is a quantity that relates the signal current i_d to the signal voltage v_d, which is called the **diode small-signal resistance**.

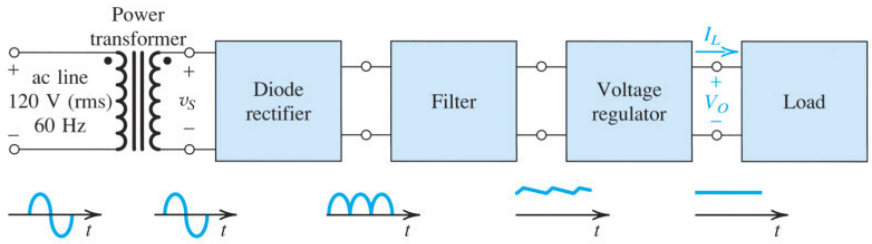
$$r_d = \frac{V_T}{I_D}$$

Procedure for Small-Signal Analysis

1. Perform DC analysis precisely using the exponential model or constant-voltage-drop model.
2. Linearize the circuit and find its small-signal equivalent.
3. Solve the linearized circuit.

4.6 Rectifier Circuits

- DV voltage must be as constant as possible in spite of variations in AC line voltage and current drawn by the load.
- First block in DC power supply is the power transformer.
  - Primary winding having N_1 turns and secondary winding having N_2 turns.
- Output of the rectifier filter still maintains a time-dependent component called **ripple**.

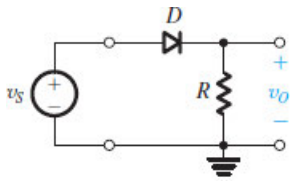


4.6.1 The Half-Wave Rectifier

$$v_O = 0 \text{ and } v_S < V_D$$

$$v_O = v_S - V_D \text{ and } v_S \geq V_D$$

- The **peak inverse voltage (PIV)** that the diode must be able to withstand without breakdown is equal to the peak of v_S.



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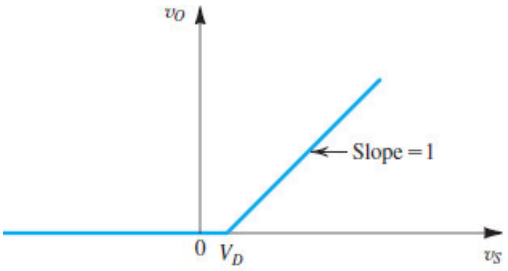

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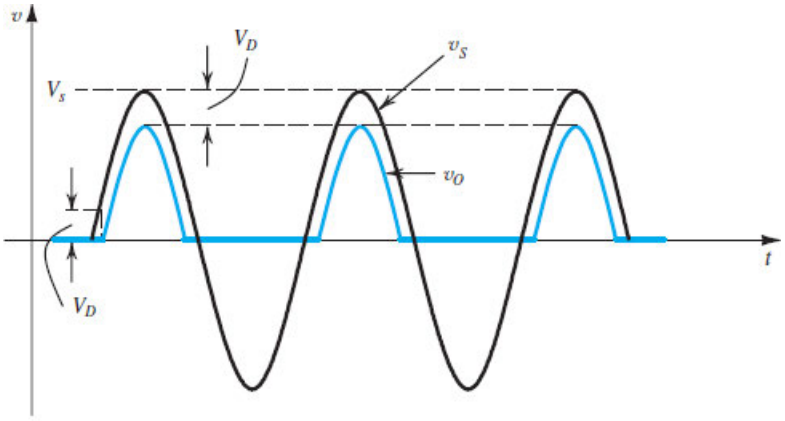

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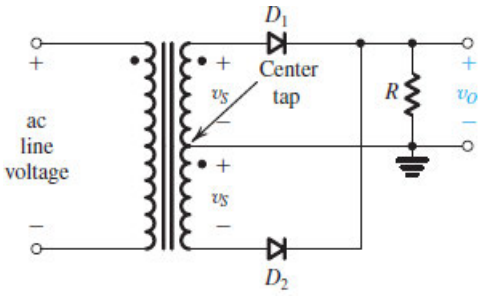
4.6.2 The Full-Wave Rectifier

- Here, the transformer secondary winding is centre-tapped to provide two equal voltages v_S across the two halves of the secondary winding.



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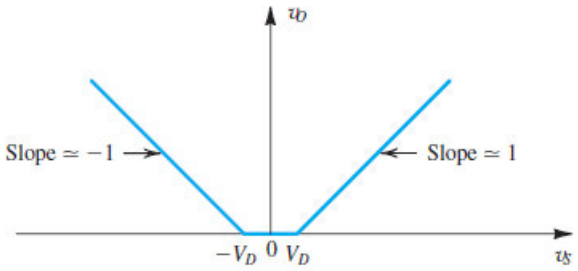

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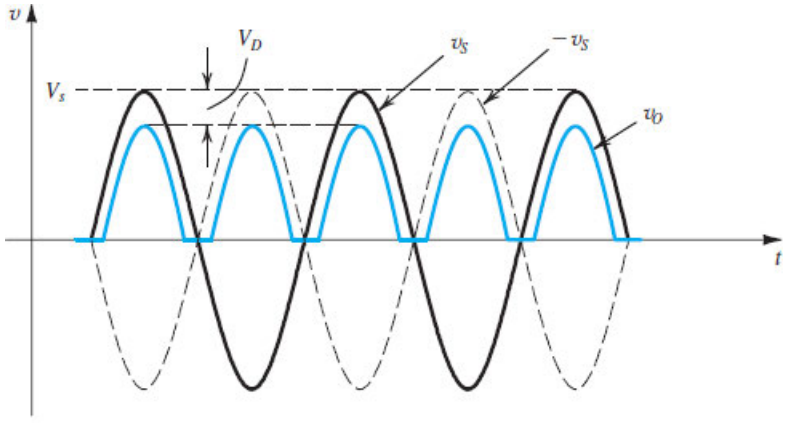
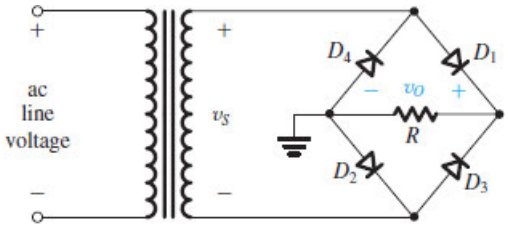


(c)

$$PIV = 2V_s - V_D$$

4.6.3 The Bridge Rectifier

- Called so because of its similarity to the Wheatstone bridge, does not require a centre-tapped rectifier, however requires four diodes.



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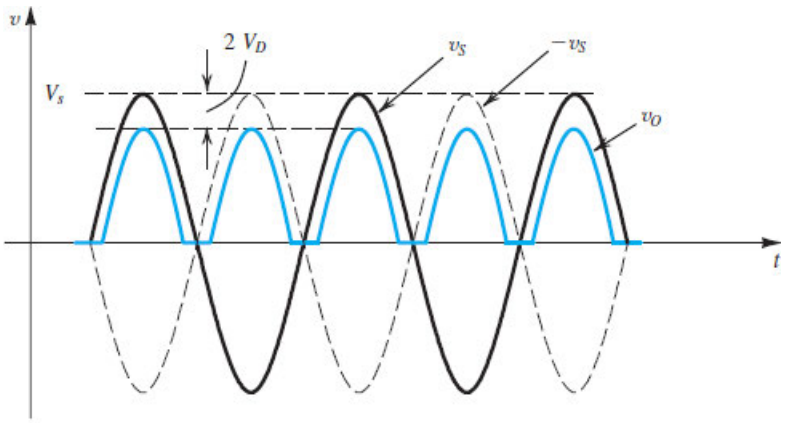
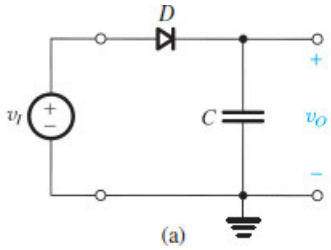


(d)

$$PIV = V_s - 2V_D + V_D = V_s - V_D$$

4.6.4 The Rectifier with a Filter Capacitor – The Peak Rectifier

- Simple way to reduce variation of output voltage is to place a capacitor across the load resistor.



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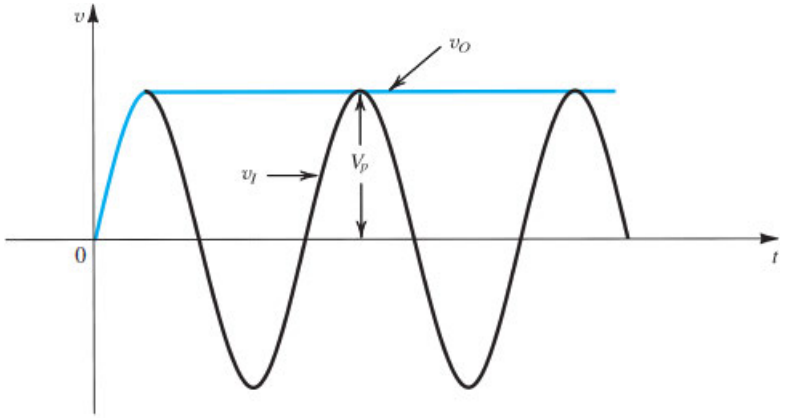
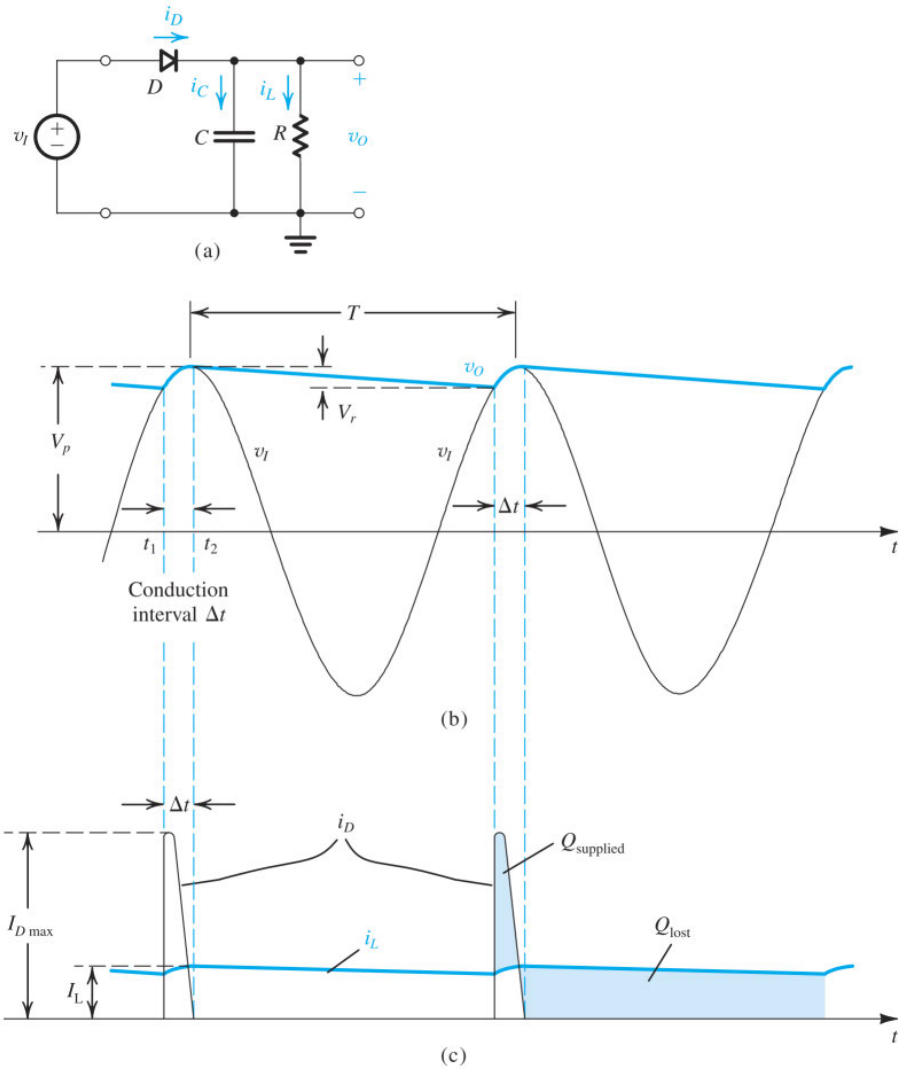


(b)

- Some observations
  - Diode conducts for a brief interval Δt near the peak of the input sinusoid and cuppies capacitor with charge equal to that lost during longer

discharge period.

- Assuming ideal diode, the diode conduction begins when $v_I \approx v_O$. We can find the value of t_2 by setting $i_D = 0$.
- During diode-off interval, the capacitor C discharges through R so v_O decays with time constant CR.
- When V_r is small, v_O is almost constant and equal to the peak value of v_I. Thus the DC output voltage is almost equal to V_p.



- Ripple voltage V_r for a half-wave rectifier is given by

$$V_r = \frac{V_p}{fCR}$$

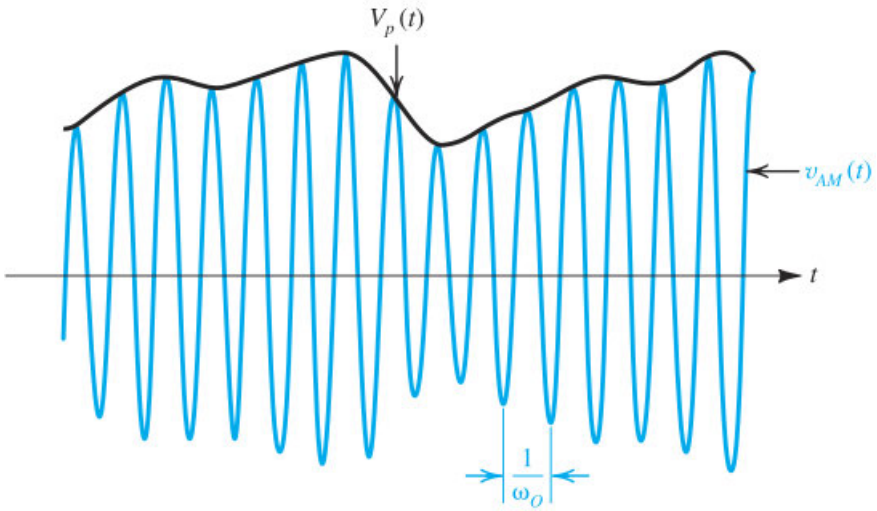
and for a peak rectifier, V_r is given by

$$V_r = \frac{V_p}{2fCR}$$

- Charge lost during the conduction time is

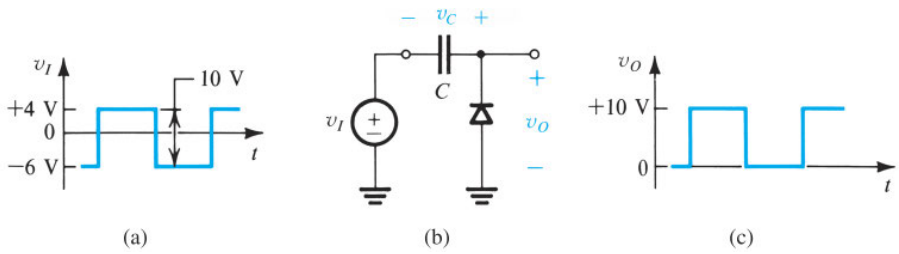
$$Q_{lost} = CV_r = I_L T$$

Amplitude Modulation



4.7 Other Diode Applications

4.7.1 The Clamped Capacitor and Bootstrapping

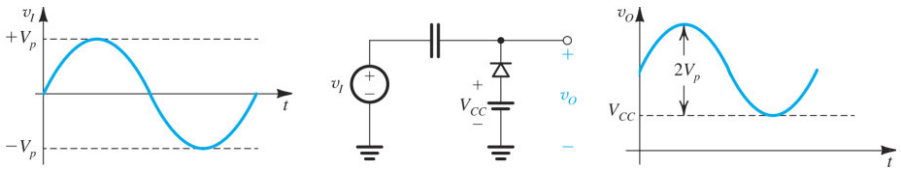


- Output voltage is given by

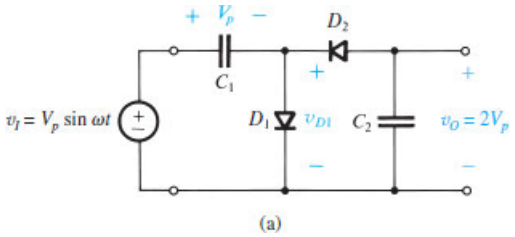
$$v_O = v_I + v_C$$

- Because the diode is connected across the output with the polarity shown, it prevents the output voltage from going below $0V$, but this connection will not constrain the positive excursion of v_O.
- The output waveform will therefore have it's lowest peak clamped to $0V$, which is why we call it a clamped capacitor.

- Average value of output waveform will not be related to average value of the input waveform at all.
- Consider pulse signal transmitted through AC-coupled system; feeding resulting pulse waveform provides it with a well-determined DC component, called DC restoration.

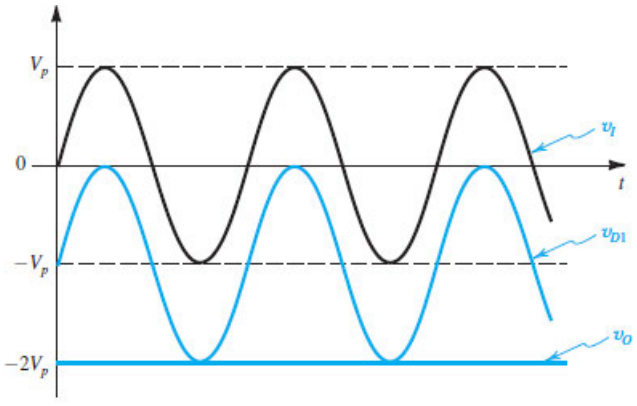


4.7.2 The Voltage Doubler



(a)

- Clamped capacitor (C_1 and D_1) in cascade with a peak rectifier (D_2 and C_2).
- While positive peaks are clamped to $0V$, negative peak reaches $-2V_p$. Because output voltage is double the input peak, the circuit is known as a voltage doubler.



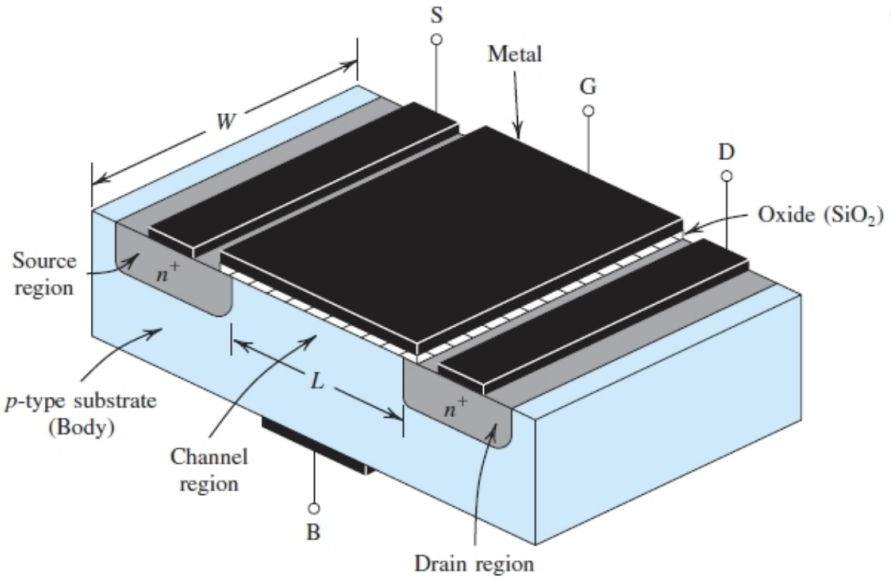
(b)

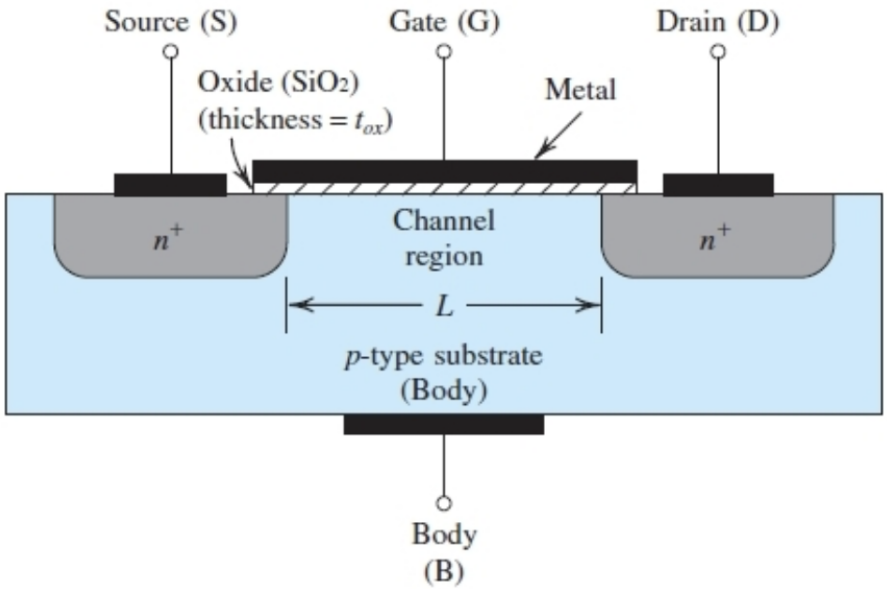
5️⃣

MOS Field-Effect Transistors

5.1 Device Structure and Physical Operation

5.1.1 Device Structure

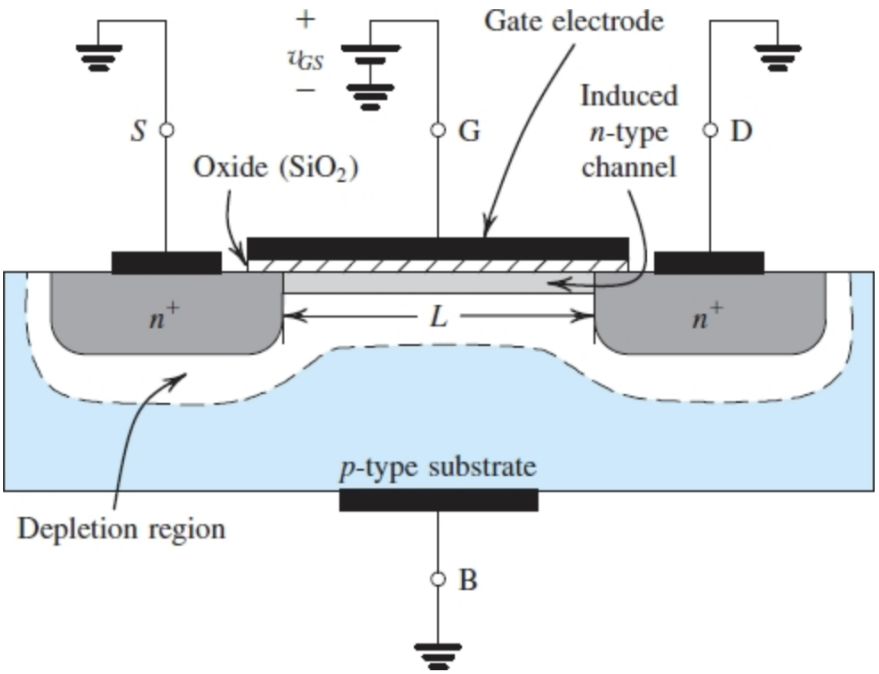




5.1.2 Operation with Zero Gate Voltage

Two back-to-back diodes in series between drain and source. Back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied.

5.1.3 Creating a Channel for Current Flow



- When voltage between drain and source is applied, current flows through induced n-region carried by mobile electrons.
- Induced region creates a channel for current flow from drain to source.
- Therefore, this transistor is called an **n-channel MOSFET**, or an **NMOS**.
- Value of v_{GS} needed for elecrons to form channel is called the threshold voltage V_t.
- **Effective** or **overdrive voltage** is given by $V_{OV} = V_{GS} - V_T$
- Oxide capacitance is capacitance of the parallel-plate capacitor per unit area

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

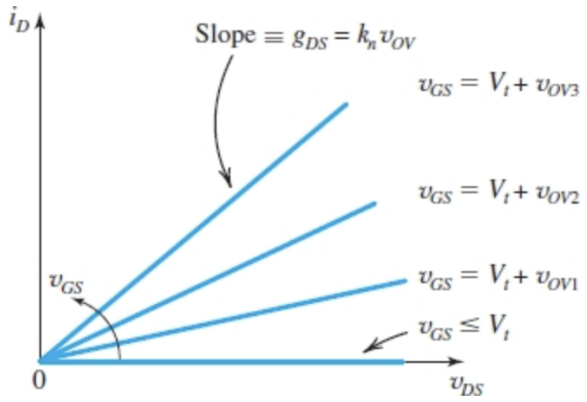
5.1.4 Applying a Small v_{DS}

- Conductance g_{DS} of the channel found from

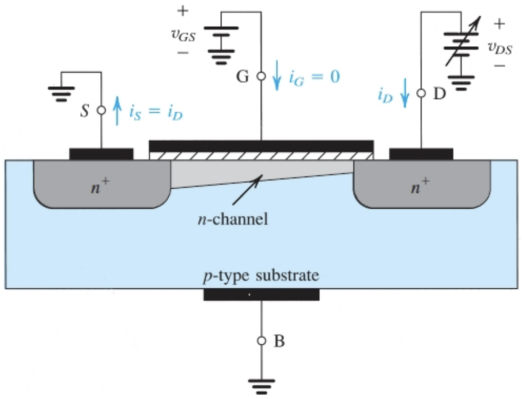
$$g_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_T)$$

- We call $k_n' = \mu_n C_{ox}$ the process transconductance parameter and $k_n = k_n'(W/L)$ the MOSFET transconductance parameter
- With v_{DS} kept small, the MOSFET behaves as a linear resistance r_{DS} whose value can be controlled by the gate voltage v_{GS}.

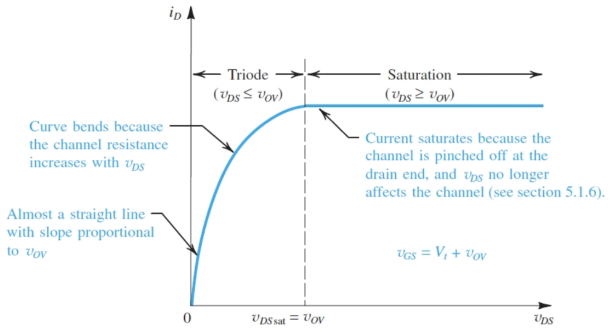
$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{k_n(v_{GS} - V_T)}$$



5.1.5 Operation as v_{DS} is Increased



- As we apply a voltage at v_{DS} we see that the channel starts to become tapered at the drain since electrons are drawn to the terminal. As we increase this voltage, the channel becomes more and more tapered.



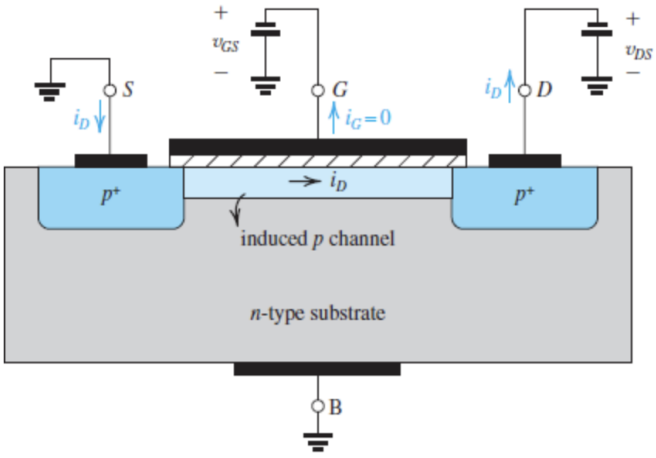
5.1.6 Operation for $v_{DS} \geq v_{OV}$: Channel Pinch-Off and Current Saturation

- As we increase v_{DS}, we see that the channel gets to a point where it is pinched off at the drain
  - For this to happen, v_{DS} must reach v_{OV} and v_{GD} must reach V_T.
- The drain current saturates at the value found by substituting $v_{DS} = v_{OV}$
- MOSFET is now in saturation region,

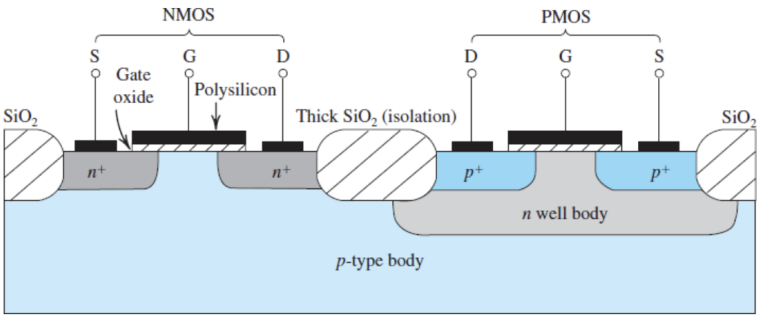
$$v_{DSsat} = v_{OV}$$

$$i_D = \frac{1}{2} k n' \left(\frac{W}{L} \right) (v_{GS} - V_T)^2$$

5.1.7 The p-Channel MOSFET

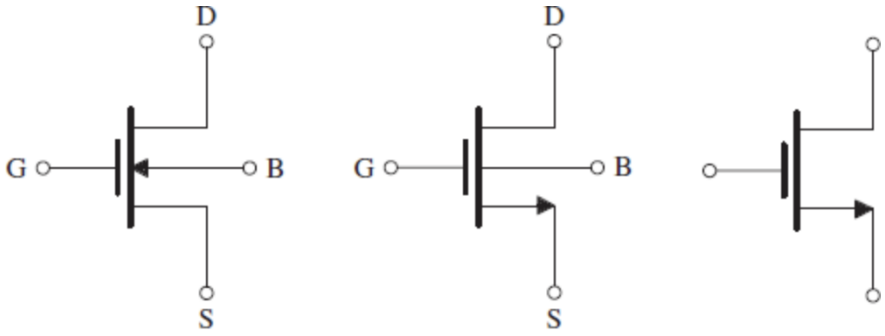


5.1.8 Complementary MOS or CMOS



5.2 Current-Voltage Characteristics

5.2.1 Circuit Symbol



5.2.2 The $i_D - v_{DS}$ Characteristics

- MOSFET has cutoff, triode, and saturation regions as discussed. Triode and cutoff are useful when we want to operate the MOSFET as a switch, and saturation is used to implement MOSFET as an amplifier.
- Boundary between triode and saturation regions (locus of saturation points) is parabolic curve given by

$$i_D = \frac{1}{2}k_n'(W/L)v_{DS}^2$$

5.2.3 The $i_D - v_{GS}$ Characteristic

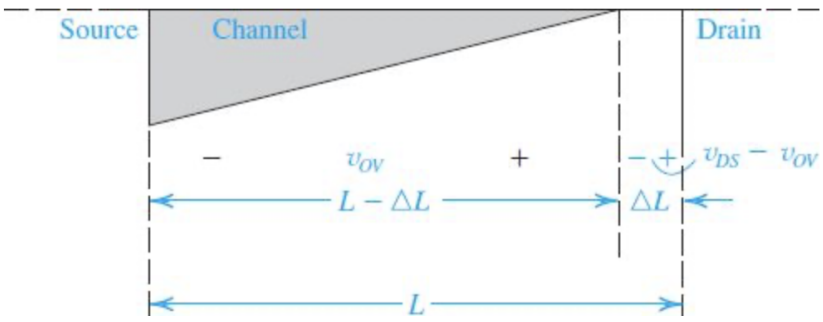
$$i_D = \frac{1}{2}k_n'(W/L)v_{OV}^2$$

5.2.4 Finite Output Resistance in Saturation

- In practice, increasing v_{DS} beyond v_{OV} does affect the channel somewhat. As v_{DS} is increased, the pinch-off point moves towards the source.

- Additional voltage added appears as a voltage drop between the narrow depletion region that gets formed.
- The channel length is essentially reduced to $L - \Delta L$, this phenomenon is called **channel-length modulation**

$$i_D = \frac{1}{2}k_n'(W/L)(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$



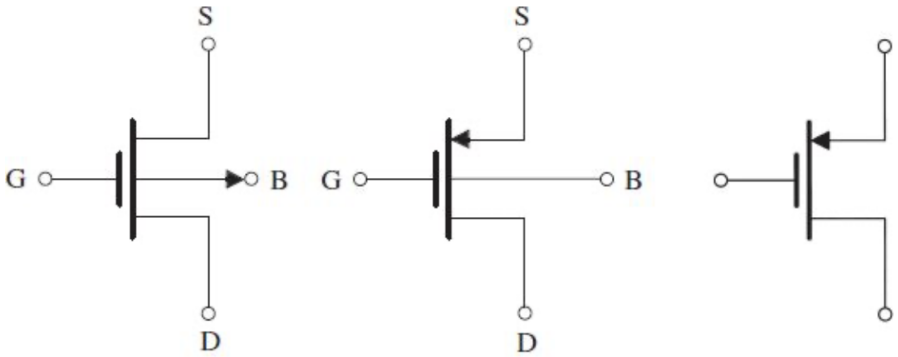
$$V_A = \frac{1}{\lambda}$$

- The voltage V_A is called the Early voltage after J.M. Early, who discovered it.
- For a change in v_{GS}, a change Δv_{DS} means a change in Δi_D. Output resistance is no longer infinite.

$$r_o = \left[\lambda \frac{k_n'}{2}\frac{W}{L}(v_{GS} - V_T)^2\right]^{-1} = \frac{V_A}{i_D'}$$

where i_D' is the drain current without channel-length modulation in account.

5.2.5 Characteristics of the p-Channel MOSFET



- In saturation, the current is given by:

$$i_D = \frac{1}{2}k_p'(W/L)(v_{SG} - |V_T|)^2\left(1 + \frac{v_{SD}}{|V_A|}\right)$$

5.3 MOSFET Circuits at DC

- Assume operating region, then solve accordingly using appropriate current equations.
- Once answers are found, check to ensure that they satisfy the requirements of the assumed operating region.

Bipolar Junction Transistors

6.1 Device Structure and Physical Operation

6.1.1 Simplified Structure and Modes of Operation

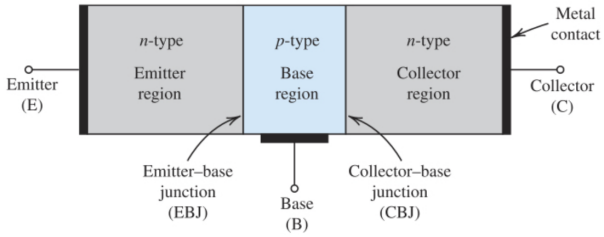


Figure 6.1 A simplified structure of the *npn* transistor.

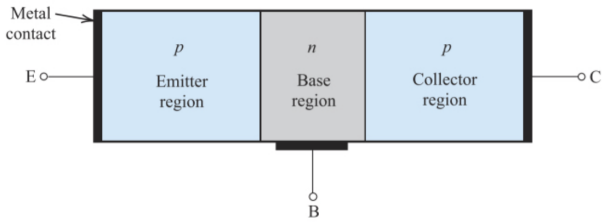


Figure 6.2 A simplified structure of the *pnp* transistor.

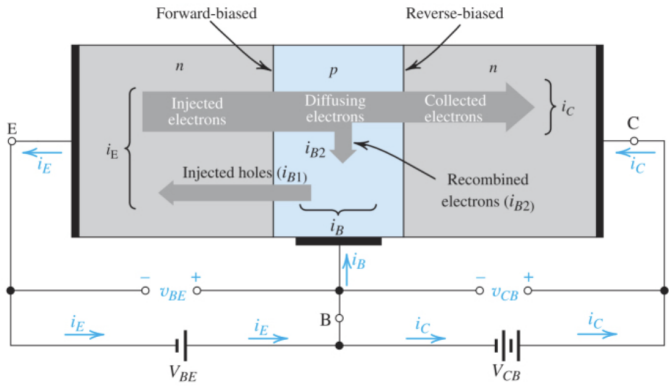
- Transistor consists of two pn junctions, called the **emitter-base junction** and the **collector-base junction**. Bias condition of each of these junctions will give us the different modes of operation.
  - Switching applications like logic circuits use **cutoff** and **saturation** modes.
  - Amplifier circuits will make use of the **active** mode.

Mode	Emitter-Base Junction	Collector-Base Junction
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

6.1.2 Operation of the npn Transistor in the Active Mode

- Two external voltage sources needed to establish active-mode.
  - Voltage V_{BE} causes p-type base to be higher in potential than n-type emitter, forward-biasing the emitter-base junction

- Voltage V_{CB} causes n-type collector to be at a higher potential than p-type base, reverse-biasing the collector-base junction.



Current Flow

- Forward bias on EBJ will cause current to flow across it, current consists of two parts
  - Electrons injected from the emitter into the base
  - Holes injected from base into the emitter.
  - Current flowing across EBJ is i_E out of the emitter terminal
- Electrons carried from emitter into the base are minority carriers in p-type region. These electrons diffuse towards the collector.
  - In this journey, some will combine with holes but most will not, as the p-type base is only lightly doped
- Collector is more positive than the base (V_{CB} reverse-biased) so the electrons sweep through, and form the current i_C.

The Collector Current

$$i_C = I_S e^{v_{BE}/V_T}$$

- i_C is independent of the magnitude of v_{CB} so long as collector is positive with respect to the base

The Base Current

- The total base current can be expressed as a fraction of the collector current i_C

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

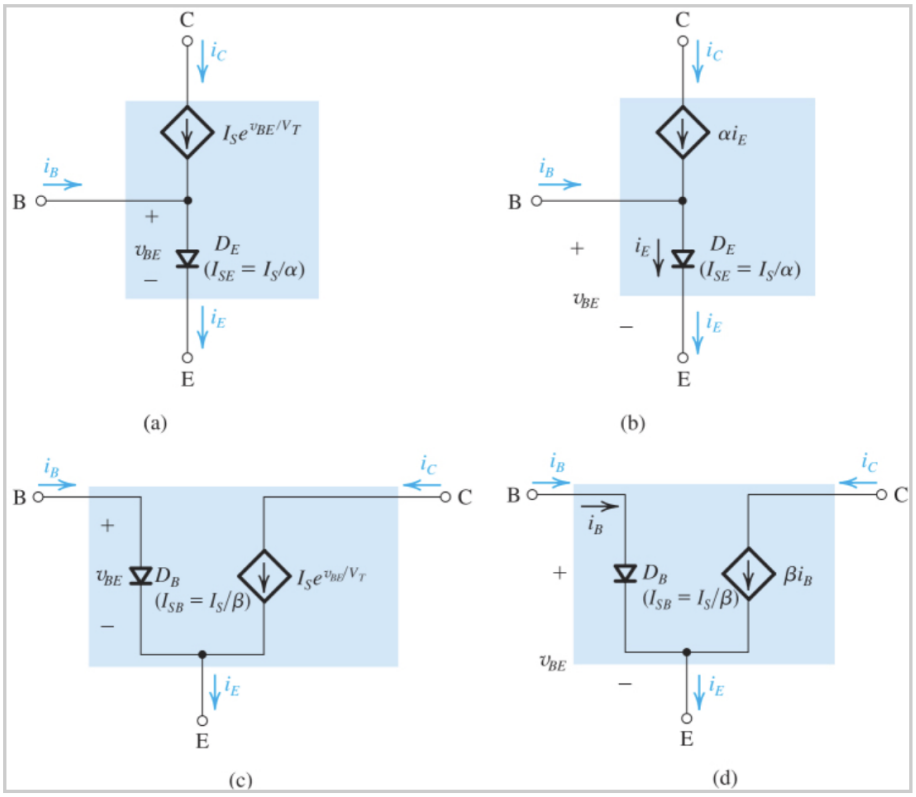
- β is a transistor parameter called the **common-emitter current gain**.

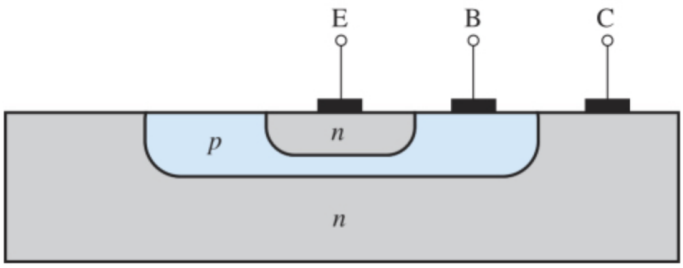
The Emitter Current

$$i_E = i_C + i_B$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

- α is called the **common-base current gain**.
- Since I_S is directly proportional to the junction area, it is also called the **scale current**.

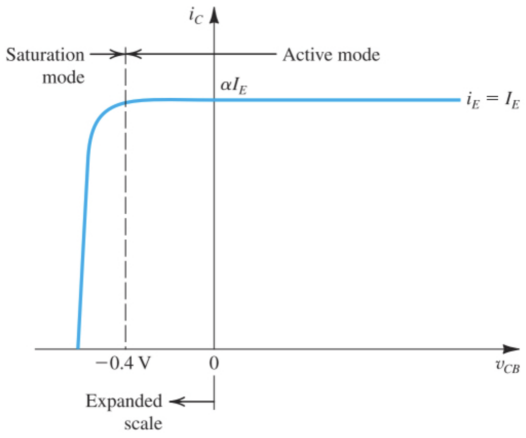




6.1.4 Operation in the Saturation Mode

- As mentioned earlier, BJT is in active mode when CBJ is reverse-biased.

- However, we know that a pn junction is not forward biased until the the voltage exceeds $0.4V$.
- Thus, we can maintain active-mode operation until $v_{CB} = -0.4V$



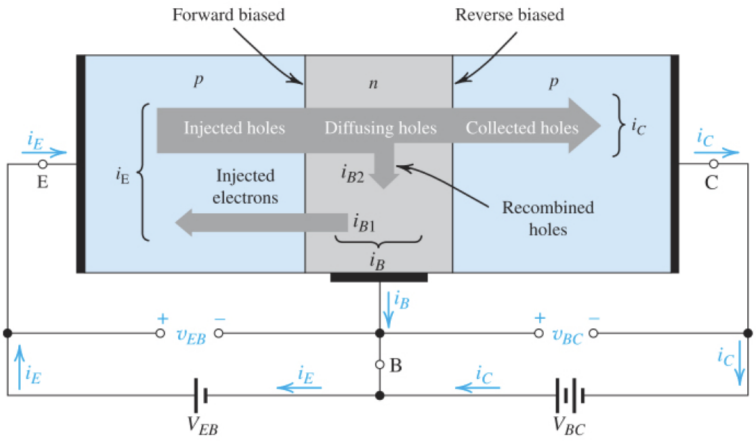
- Let us consider the equations for i_C and i_B

$$i_C = I_S e^{v_{BE}/V_T} - I_{SC} e^{v_{BC}/V_T}$$

$$i_B = (I_S/\beta) e^{v_{BE}/V_T} + I_{SC} e^{v_{BC}/V_T}$$

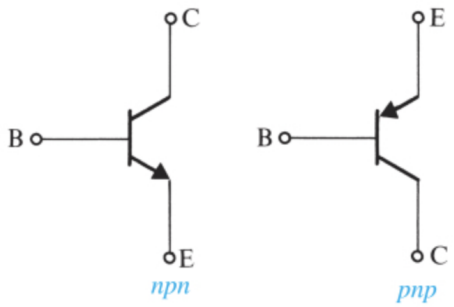
- We see that this ratio is lower than the value of β, and it decreases further as v_{BC} is increased and transistor goes deeper into saturation.
  - This ratio is known as β_{forced}
- We can determine if the BJT is in saturation mode by either of the following two tests:
  - Is the CBJ forward biased by more than $0.4V$?
  - Is the ratio i_C/i_B lower than β?
- We assume that a transistor at the edge of saturation has $V_{CEsat} = 0.3V$ and a transistor deep in saturation has $V_{CEsat} = 0.2V$.

6.1.5 The pnp Transistor

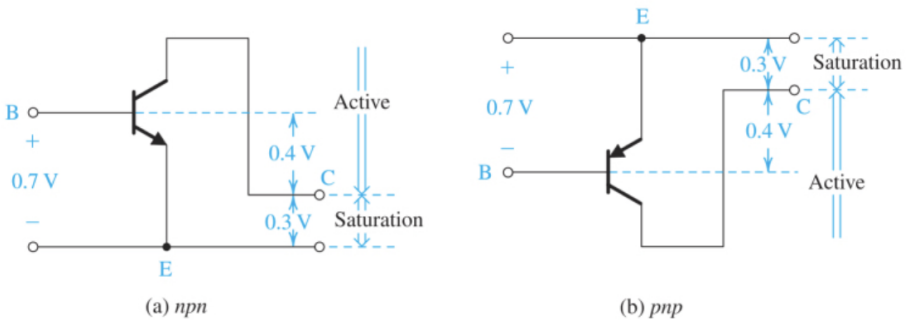


6.2 Current-Voltage Characteristics

6.2.1 Circuit Symbols and Conventions

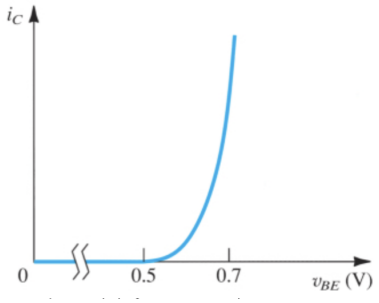


- We see that a transistor whose EBJ is forward-biased (usually $0.7V$) will operate in the active mode as long as collector voltage does not fall below that of base by more than $0.4V$.
  - Otherwise the transistor will enter the saturation region.
- The pnp transistor will operate in the active mode if the EBJ is forward-biased (usually $0.7V$) and the collector voltage is not allowed to rise above base voltage by more than $0.4V$ or so.
  - Otherwise the pnp transistor will enter the saturation region.



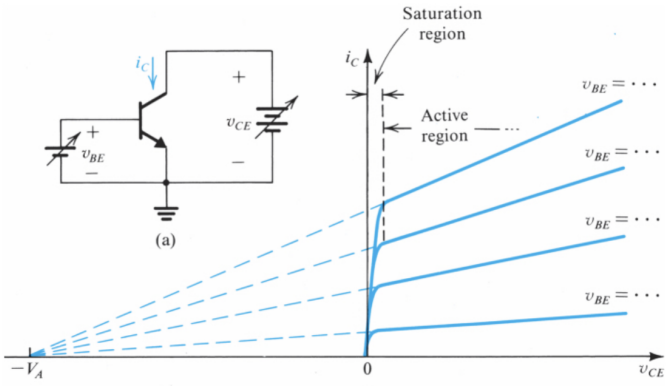
6.2.2 Graphical Representation of Transistor Characteristics

$$i_C = I_S e^{v_{BC}/V_T}$$



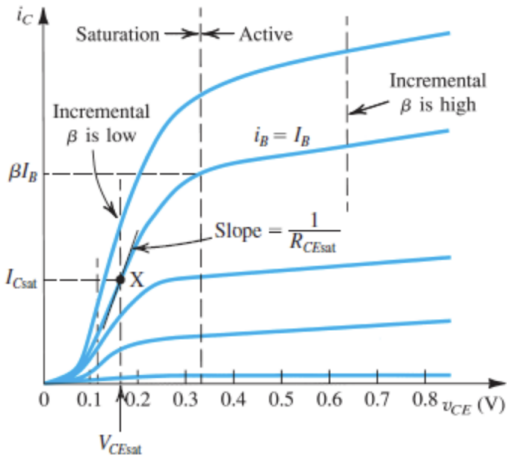
6.2.3 Dependence of i_C on the Collector Voltage — The Early Effect

- In active region, collector current of a practical BJT shows some dependence on the collector voltage.
- The transistor is connected in the common-emitter configuration.
- At each value of v_{BE}, the corresponding $i_C - v_{CE}$ characteristic curve can be measured point by point by varying the DC source connected between collector and emitter and measuring the corresponding collector current.
- The result is the family characteristic curves known as common-emitter characteristics.



$$r_o = \frac{V_A + V_{CE}}{I_C}$$

6.2.4 An Alternative Form of the Common-Emitter Characteristics



6.3 BJT Circuits at DC

- Assume operating region, then solve accordingly using appropriate current equations.
- Once answers are found, check to ensure that they satisfy the requirements of the assumed operating region.

7️⃣

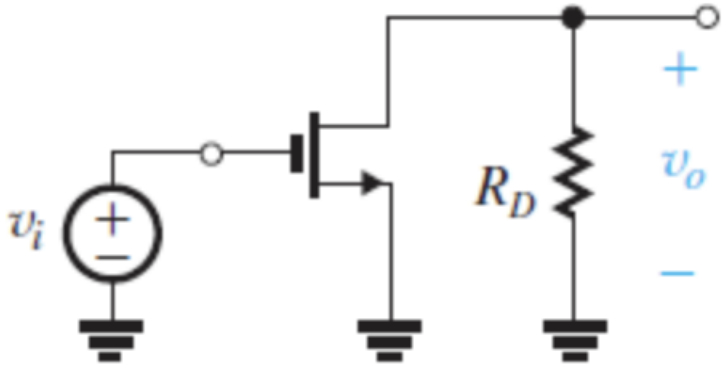
Transistor Amplifiers

7.3 Basic Configuration

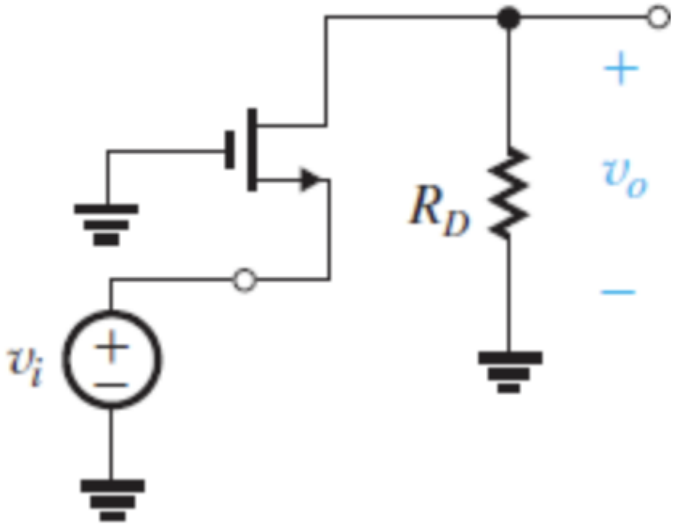
- By biasing the circuit to an appropriate point and by keeping input signal (v_{gs} or v_{be}) small, we can achieve almost-linear amplification
- Discrete-circuit amplifiers can be constructed using discrete components.

7.3.1 The Three Basic Configurations

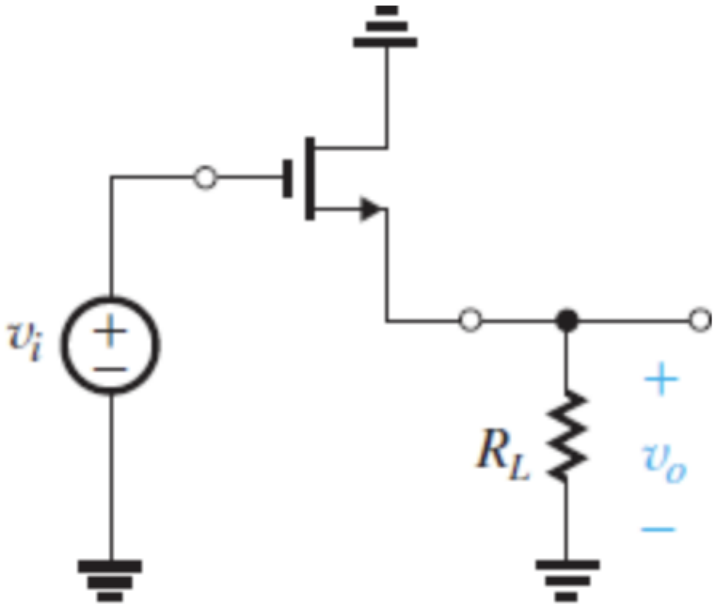
Common Source



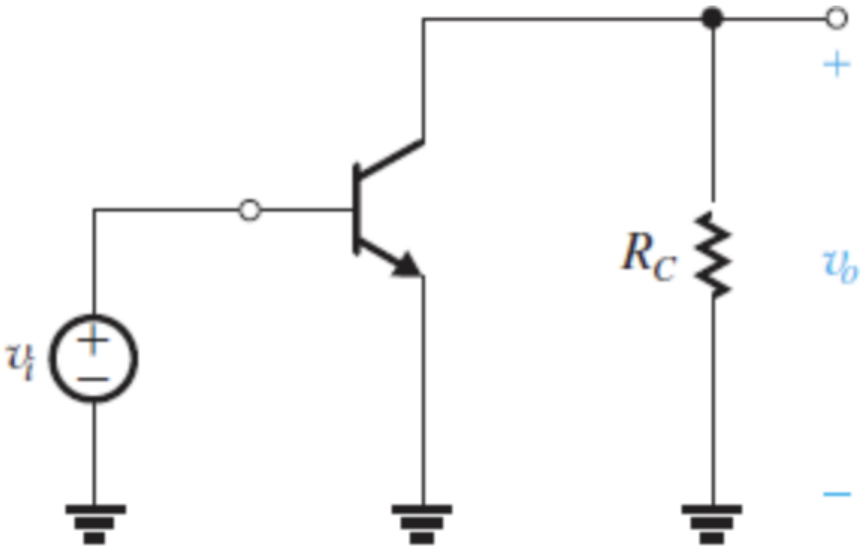
Common Gate



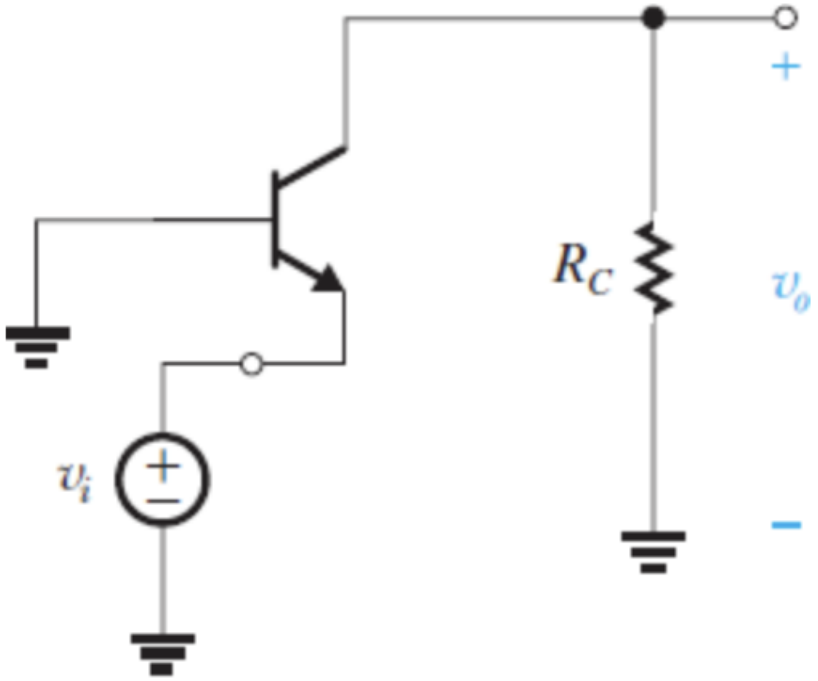
Common Drain



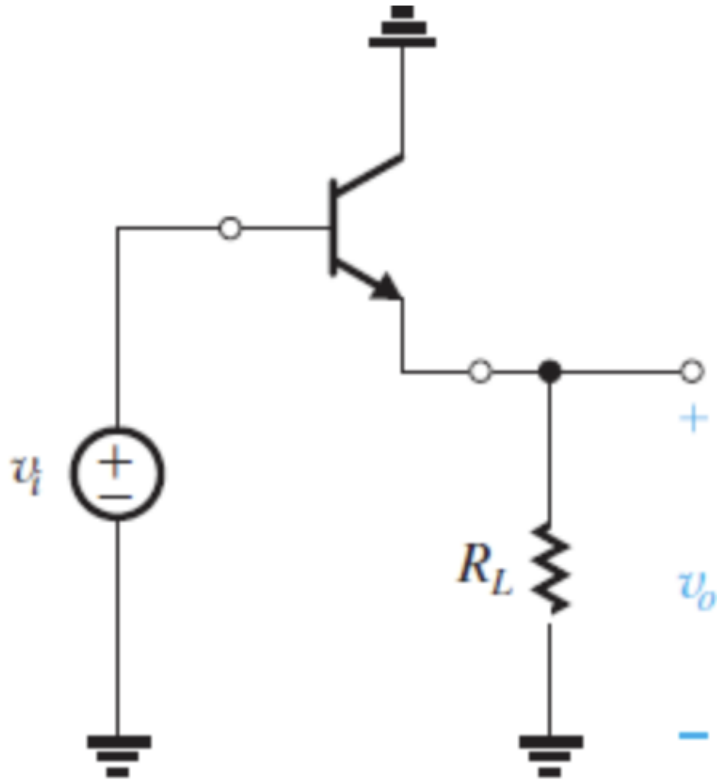
Common Emitter



Common Base

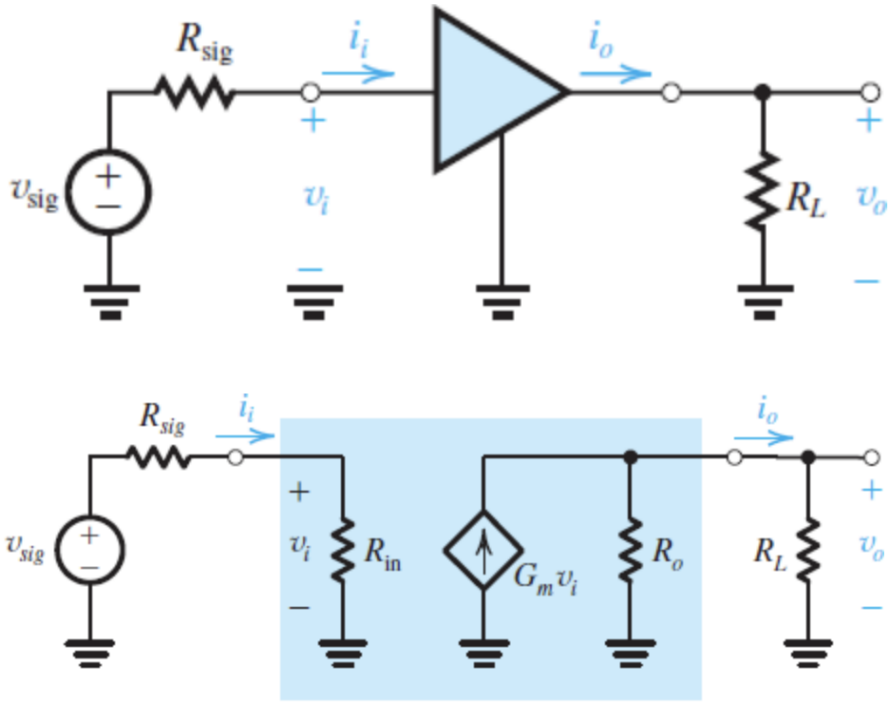


Common Collector



- We see that the circuit is named common to whichever terminal is connected to the ground.

7.3.2 Characterizing Amplifiers



- Input resistance R_{in} represents the loading effect of the input on the signal source.

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig}$$

- Open-circuit voltage gain given by $A_{vo} = \frac{v_o}{v_i}$ as $R_L \to \infty$
- The voltage gain of the amplifier proper

$$A_v = A_{vo} \frac{R_L}{R_L + R_o}$$

- and the overall voltage

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_{vo} \frac{R_L}{R_L + R_o}$$

7.3.3 Common-Source and Common-Emitter Amplifiers

- Overall voltage gain of the common-source amplifier

$$G_v = -g_m(R_D||R_L)$$

- Overall voltage gain of the common-emitter amplifier

$$G_v = -\frac{r_\pi}{r_\pi + R_{sig}} g_m(R_C||R_L)$$

- Final remarks
  - Most useful of all the amplifiers — exhibit moderate-to-high input resistance, moderate-to-high output resistance, and high voltage gain.
  - Input resistance of the CE is $r_\pi = \beta/g_m$ is inversely proportional to I_C

7.3.4 Common-Source/Emitter with Source/Emitter Resistance

$$v_{gs} = \frac{v_i}{1 + g_m R_s}$$

- We can derive the expression for the input resistance

$$R_{in} = (\beta + 1)(r_e + R_e)$$

- The **resistance-reflection rule** states that the input resistance looking into the base is $(\beta + 1)$ times higher than the total resistance in the emitter.

7.3.5 Common-Gate and Common-Base Amplifiers

$$G_v = \frac{R_D||R_L}{R_{sig} + 1/g_m}$$

7.3.6 Source and Emitter Followers

- Why do we need voltage buffers?
  - Between input and output resistance, we lose a lot of the input voltage
  - However, in the source/emitter followers, we see that we can return most our voltage back, making it possible to implement the unity-gain amplifiers.

The Source Follower

- Characteristic properties of the source follower
  - $R_{in} = \infty$
  - $A_{vo} = 1$
  - $R_o = 1/g_m$

- Voltage at the source terminal will follow that of the input
- Source follower is also used as the output (last) stage in a multistage amplifier where it’s function is to make output resistance of the overall amplifier low
  - This enables the amplifier to supply lots of current to the amplifier without loss of gain.

The Emitter Follower

$$i_e = \frac{v_i}{r_e + R_L}$$

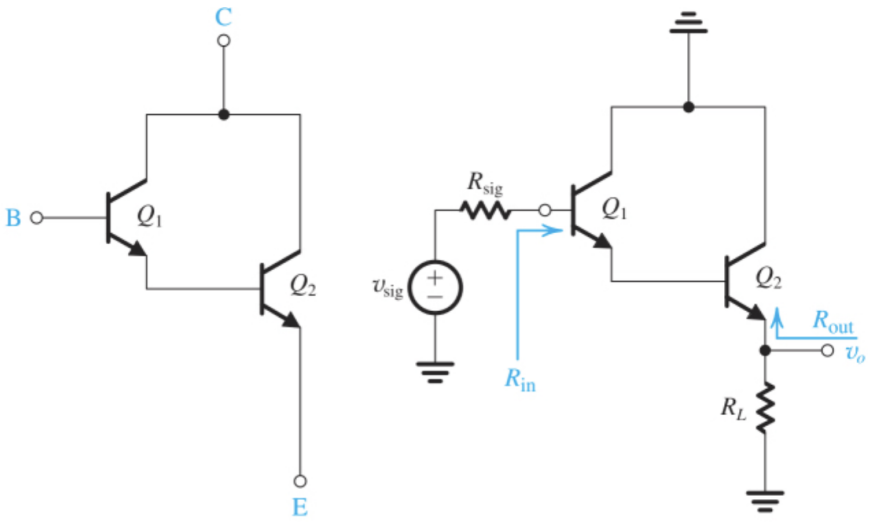
$$R_{in} = (\beta + 1)(r_e + R_L)$$

- The emitter follower takes the low load resistance and reflects it by $(\beta + 1)$ to the base side.

$$G_v = \frac{(\beta + 1)R_L}{(\beta + 1)R_L + (\beta + 1)r_e + R_{sig}}$$

Darlington Configuration

- We can improve the emitter follower by placing two BJTs in cascade



7.3.7 Summary Tables and Comparisons

- MOSFETs provide higher (ideally infinite) input resistances (except CG), advantage over BJTs
- BJTs have higher g_m values, resulting in higher gains

- BJT remains component of choice for discrete-circuit amplifiers as they’re easier to handle
- IC amplifiers use MOSFET amplifiers
- CS and CE configurations best for realizing bulk of the gain required in an amplifier

7.3.8 When and How to Include Output Resistance r_o

- In IC amplifier design and analysis, r_o must always be taken into account
- In other instances, we can usually safely ignore the effects of r_o as it will not affect our results that much

7.4 Biasing

- Important step in trans amp design is selecting appropriate DC operating point
- Second consideration is to locate a DC operating point that allows us to get high voltage gain while ensuring output voltage swing does not force the transistor out of active region (avoid nonlinear distortion)

7.4.1 The MOSFET Case

Biasing by Fixing V_{GS}

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

Biasing by Fixing V_G and Connecting a Resistance in the Source

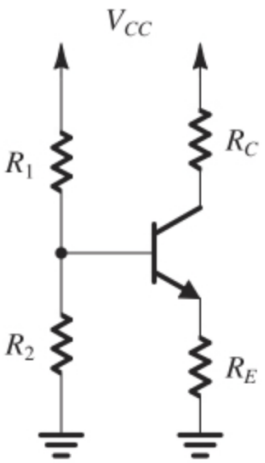
$$V_G = V_{GS} + R_S I_D$$

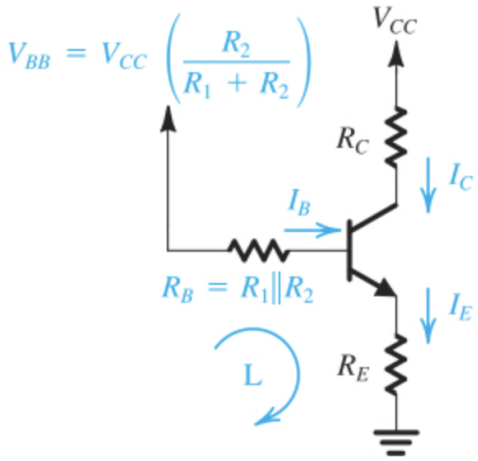
Biasing Using a Drain-to-Gate Feedback Resistor

$$V_{DD} = V_{GS} + R_D I_D$$

7.4.2 The BJT Case

The Classical Discrete-Circuit Bias Arrangement

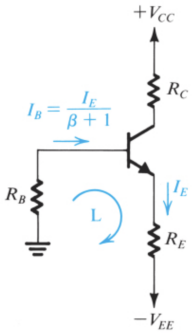




$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta + 1)}$$

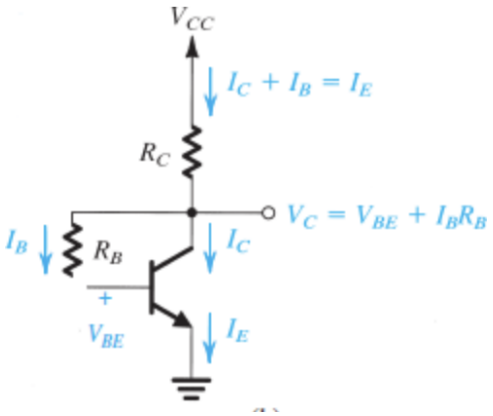
A Two-Power-Supply Version of the Classical Bias Arrangement

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta + 1)}$$



Biasing Using a Collector-to-Base Feedback Resistor

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/(\beta + 1)}$$



7.5 Discrete-Circuit Amplifiers

- Circuits in this section use large caps (think μF range) to couple signal source to amplifier input and couple amplifier output to another amp input.
- SInce caps block DC, we can first carry out the bias design then connect the signal source and load without disturbing it.
  - These are called **capacitively-coupled amplifiers**.